Project Abstract

(VI)sualizer: A Smart Electronic Load

An instrument for profiling solar, chemical, and grid-powered energy delivery devices

Entry # NXP3767

Submitted to

Circuit Cellar

for

The NXP mbed Design Challenge

Introduction

This document describes the "(VI)sualizer" -- a lab instrument for profiling solar, chemical, and grid-powered energy delivery devices.

The (VI)sualizer gets its name from the fact that it allows the user to examine – or visualize -- the voltage (V) and current (I) delivery ability of an energy source. It can calculate the load resistance into which a solar cell delivers maximum power, or measure and capture the Amp-hour capacity of a battery, or, using pulsatile loads, test the voltage regulation accuracy of a conventional power supply.

By including the signal generation, testing algorithms, and data capture/storage functions in a single instrument, the (VI)sualizer offers an advantage over lash-ups using several pieces of commercially available gear to achieve the same results.

Hardware overview

Figure 1 illustrates the main components of the (VI)sualizer. An mbed module accepts input data from the local and/or remote interfaces, commands the desired load current, and monitors operating conditions to protect against over stress.

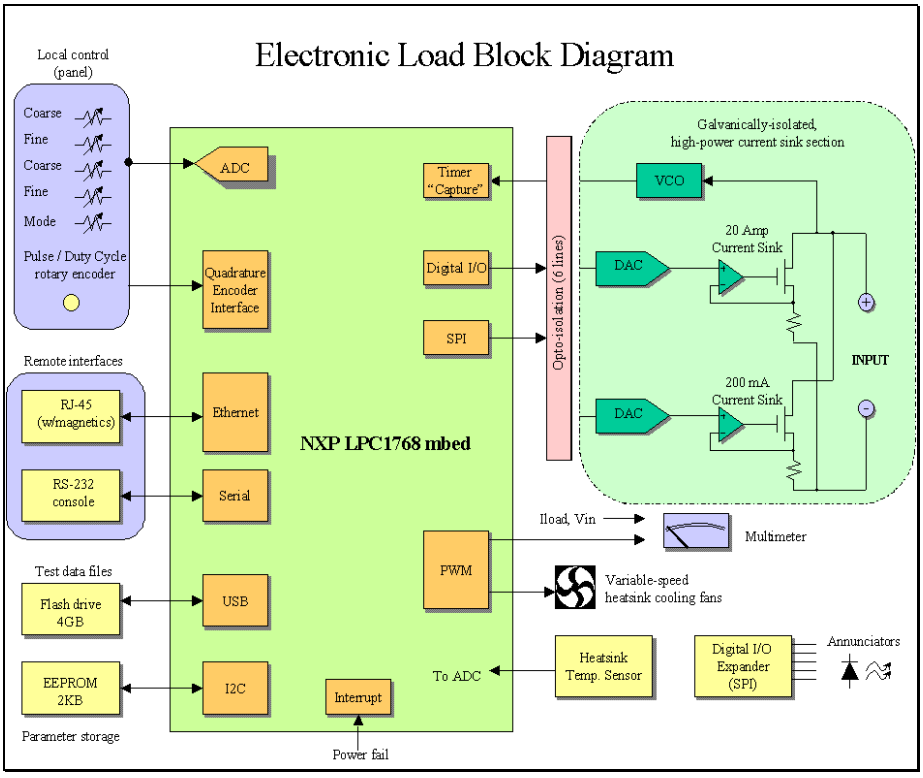


Figure 1 - Block Diagram

The load current is controlled by a bank of power MOSFETs mounted on fan-cooled heat sinks, controlled by a DAC/op-amp drive circuit that is used to set the target current. The DACs are driven through an optical isolation interface.

A voltage-controlled oscillator is used to sense the applied voltage. Its output is also optically isolated.

Two storage devices augment the mbed's native storage: one, a 4GB flash memory (USB flash drive) for test data files and the other a small EEPROM for parameter storage.

A meter shows current, voltage, wattage, and pulse values. Some signals are generated by PWM outputs on the mbed; the others come directly from hardware.

Another PWM signal drives the variable-speed cooling fans, according to the temperature reading reported by a sensor attached to the heat sink.

Software Overview
The main modules of the firmware are a main task loop that implements a cooperative multi-tasking executive; a collection of state-machine-like task modules that handle the test algorithms; and interrupt handlers that control data capture and pulse generation.

The remote user interface comprises five html/Javascript web pages. They rely on RPC calls to invoke functions on the mbed. Those functions return data to the browser by means of a JSON-compatible string.

Also, two new drivers were written in C++ especially for this project: one for the QEI hardware, and one for Timer 2 "Capture" inputs. A snippet of the Capture driver is shown below:

```
/**************************************************************************//**
 * @brief        Create a Capture object and configure it.
 * @param pin    Selects p30 or p29 as the Capture input
 * @return        None
 *****************************************************************************/
Capture::Capture(PinName pin)
{
    #define DEFAULT_PCLK_DIV    PCLK_DIV_4          // Default to PCLK/4 (24MHz)
    #define DEFAULT_EDGE        CAP_EDGE_RISE       // Default to the rising edge
    #define DEFAULT_INT_MODE    CAP_INT_ON          // Default to interrupts on

    /* Set up clock and power, using default PCLK divider choice */
    LPC_SC->PCONP |=  PCONP_PCTIM2;     // Turn on the power to the  timer
    LPC_SC->PCLKSEL1 =  (LPC_SC->PCLKSEL1 & ~PCLKSEL1_PCLK_TIMER2_MASK) | (DEFAULT_PCLK_DIV << 12 );


    /* Assign the capture pin. Use a pull-up. Also select capture edge and int mode     */
    switch (pin) {
        case p30:
                channel = 0;
                // Enable pin 30 for CAP 2.0
                LPC_PINCON->PINSEL0 = (LPC_PINCON->PINSEL0 & PINSEL0_CAP20_MASK) | PINSEL0_CAP20 ;
                LPC_PINCON->PINMODE0 = (LPC_PINCON->PINMODE0 & PINMODE0_CAP20_MASK) | PINMODE0_CAP20;
                // Select the capture edge and int mode
                LPC_TIM2->CCR = ( LPC_TIM2->CCR & ~((uint32_t)0x7) ) | DEFAULT_EDGE | (DEFAULT_INT_MODE << 2);
            break;
        case p29:
                channel = 1;
                // Enable pin 29 for CAP 2.1
                LPC_PINCON->PINSEL0 = (LPC_PINCON->PINSEL0 & PINSEL0_CAP21_MASK) | PINSEL0_CAP21 ;
                LPC_PINCON->PINMODE0 = (LPC_PINCON->PINMODE0 & PINMODE0_CAP21_MASK) | PINMODE0_CAP21;
                // Select the capture edge and int mode
                LPC_TIM2->CCR = ( LPC_TIM2->CCR & ~((uint32_t)0x38) ) | (DEFAULT_EDGE <<3) | (DEFAULT_INT_MODE << 5);
            break;
```

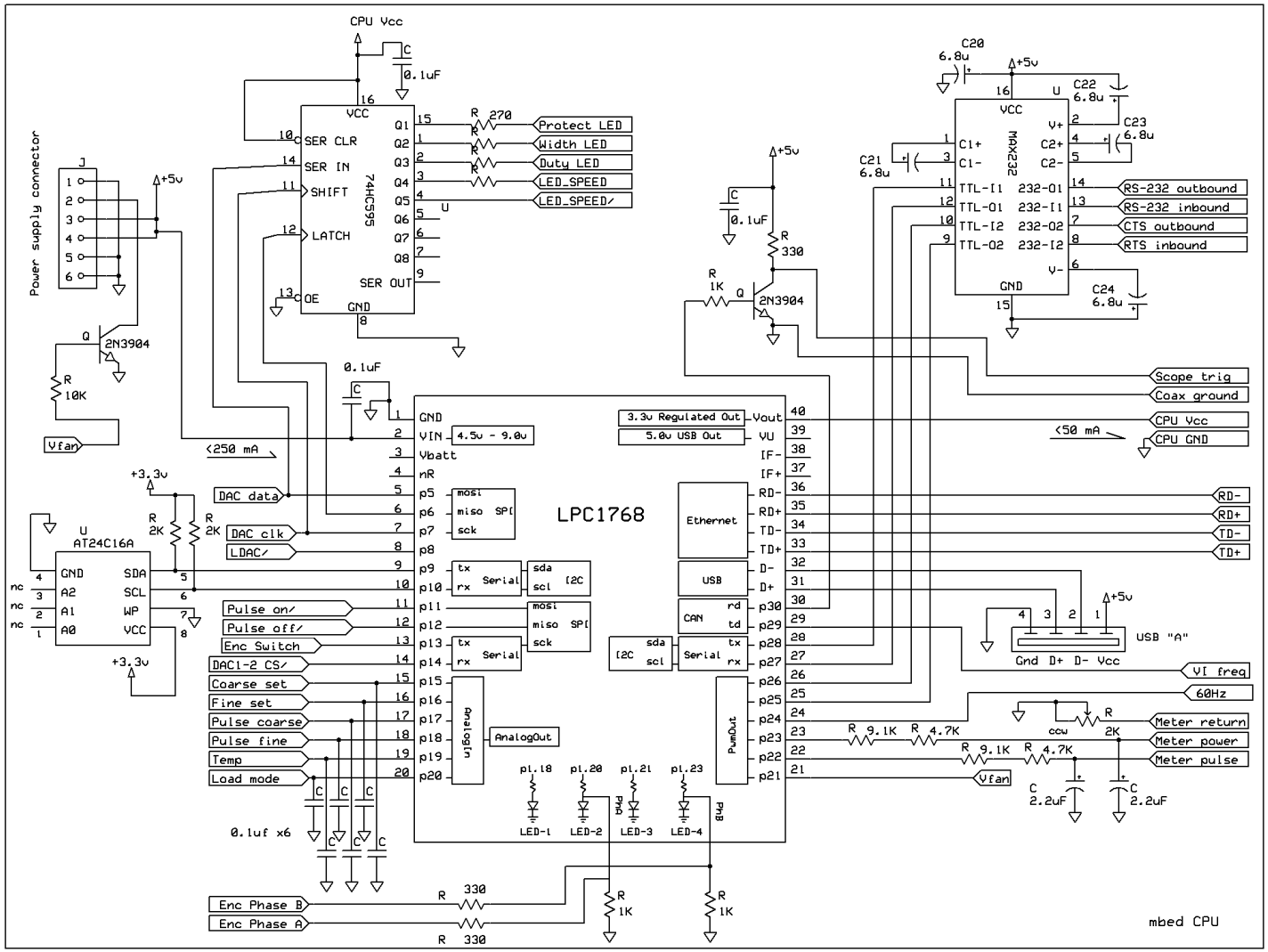
Altogether, the software and libraries take up about 135 kB of Flash, and about 8 kB of RAM.

Summary
Every major module of the mbed was used (save for the CAN module, which was not required). All I/O pins were used – in fact, an SPI port expander was used to generate five extra digital outputs. Some 13 mbed Handbook functions were used, along with 4 Cookbook functions and 2 of my own.

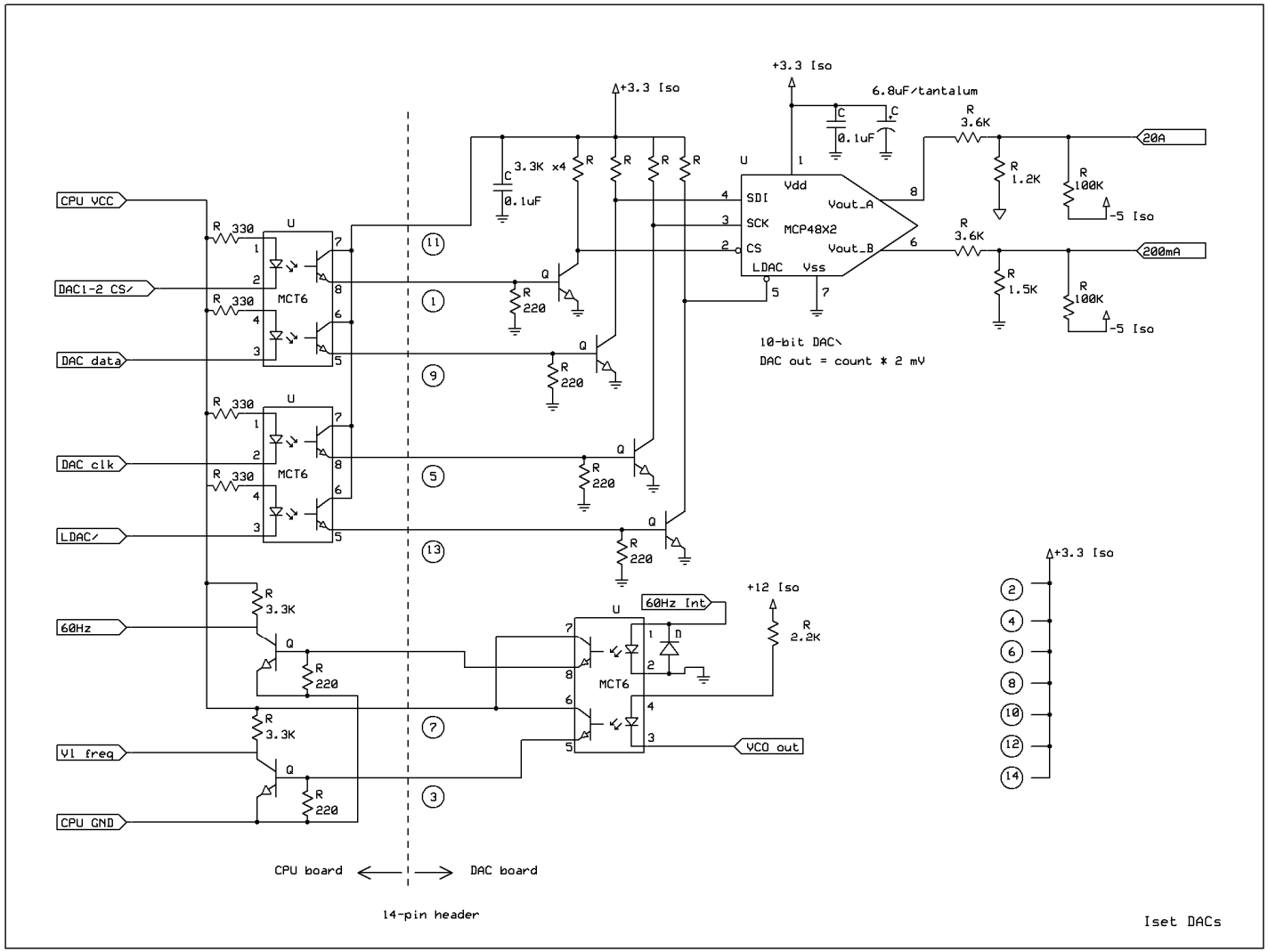
All together, the mbed hardware and software provided an excellent environment for the development of this project.

I can truly say that bringing this design to the same level of complexity would not have been possible in the same time frame had I used a bare-metal processor without the full range of software provided to mbed users.

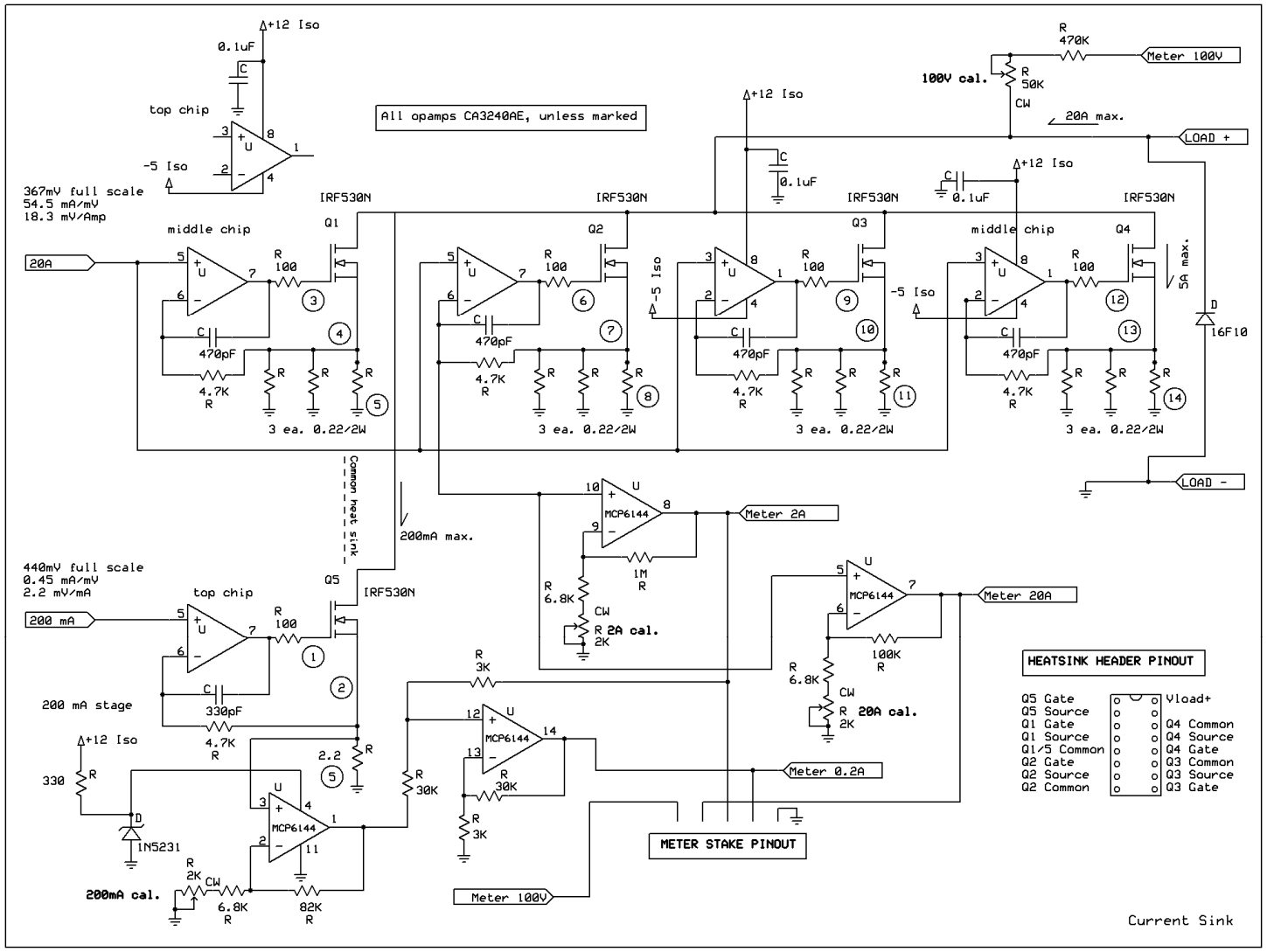
Mbed CPU


CPU Vcc
0.1uF
74HC595
SER CLR
SER IN
SHIFT
LATCH
OE
SER OUT
Protect LED
Width LED
Duty LED
LED_SPEED
LED_SPEED/
Power supply connector
2N3904
10K
Vfan
<250 mA
+3.3v
+5v
DAC data
DAC clk
LDAC/
AT24C16A
Pulse on/
Pulse off/
Enc Switch
DAC1-2 CS/
Coarse set
Fine set
Pulse coarse
Pulse fine
Temp
Load mode
0.1uf x6
Enc Phase B
Enc Phase A
330
1K
LPC1768
4.5v - 9.0v
Ybatt
3.3v Regulated Out
5.0v USB Out
Ethernet
USB
CAN
Serial
SPI
I2C
AnalogIn
AnalogOut
PwmOut
LED-1
LED-2
LED-3
LED-4
C20
6.8u
C21
6.8u
C22
6.8u
C23
6.8u
C24
6.8u
MAX232
TTL-I1
TTL-O1
TTL-I2
TTL-O2
232-O1
232-I1
232-O2
232-I2
RS-232 outbound
RS-232 inbound
CTS outbound
RTS inbound
Scope trig
Coax ground
CPU Vcc
CPU GND
<50 mA
RD-
RD+
TD-
TD+
USB "A"
Gnd D+ D- Vcc
VI freq
60Hz
Meter return
Meter power
Meter pulse
9.1K
4.7K
ccw
2K
2.2uF
mbed CPU

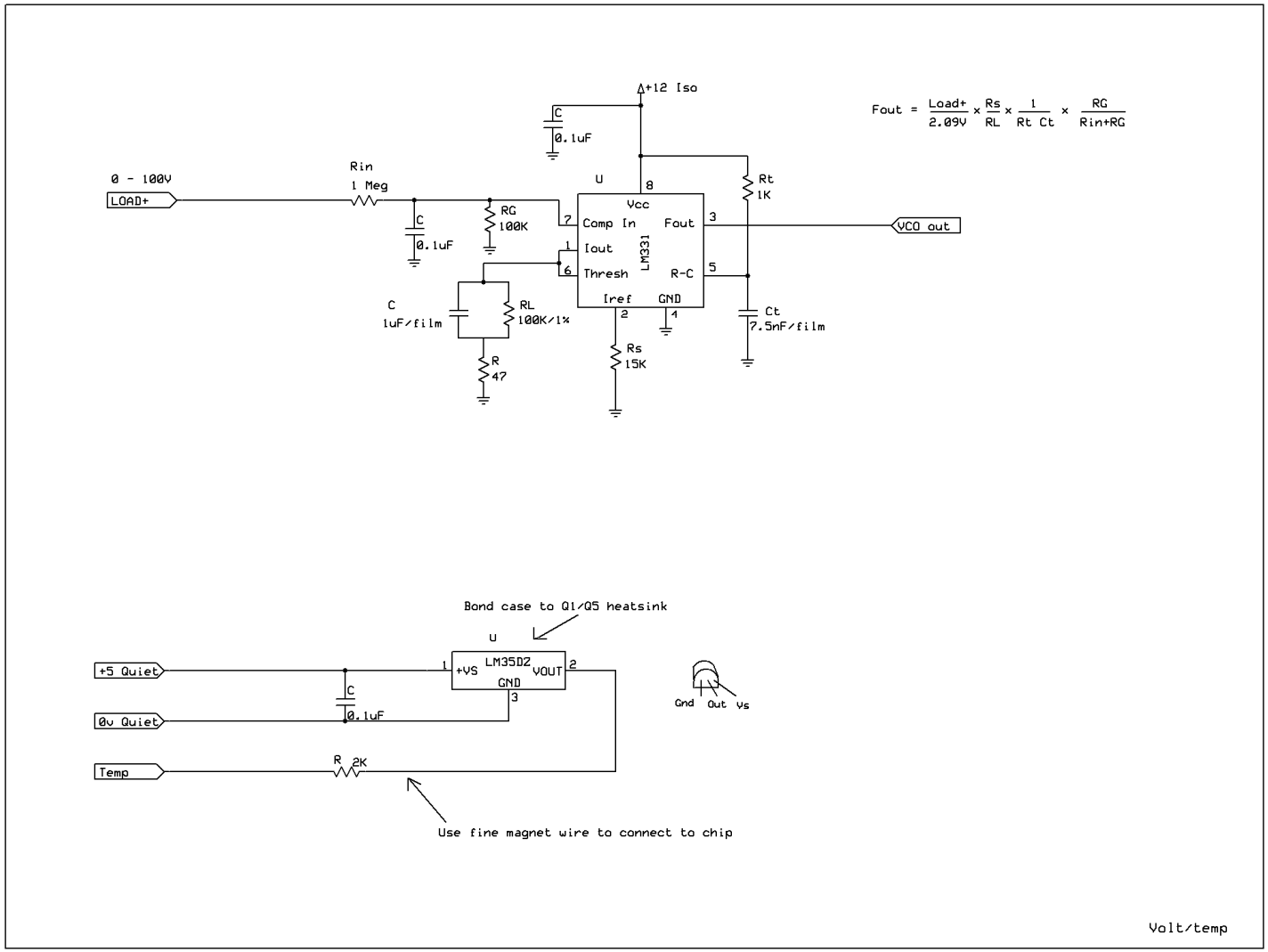
Iset DACs


+3.3 Iso
6.8uF/tantalum
3.3K x4
0.1uF
MCP48X2
SDI
SCK
CS
LDAC
Vdd
Vss
Vout_A
Vout_B
10-bit DAC
DAC out = count * 2 mV
20A
200mA
-5 Iso
CPU VCC
DAC1-2 CS
DAC data
DAC clk
LDAC
60Hz
Y1 freq
CPU GND
MCT6
60Hz Int
+12 Iso
VCO out
CPU board
DAC board
14-pin header
Iset DACs

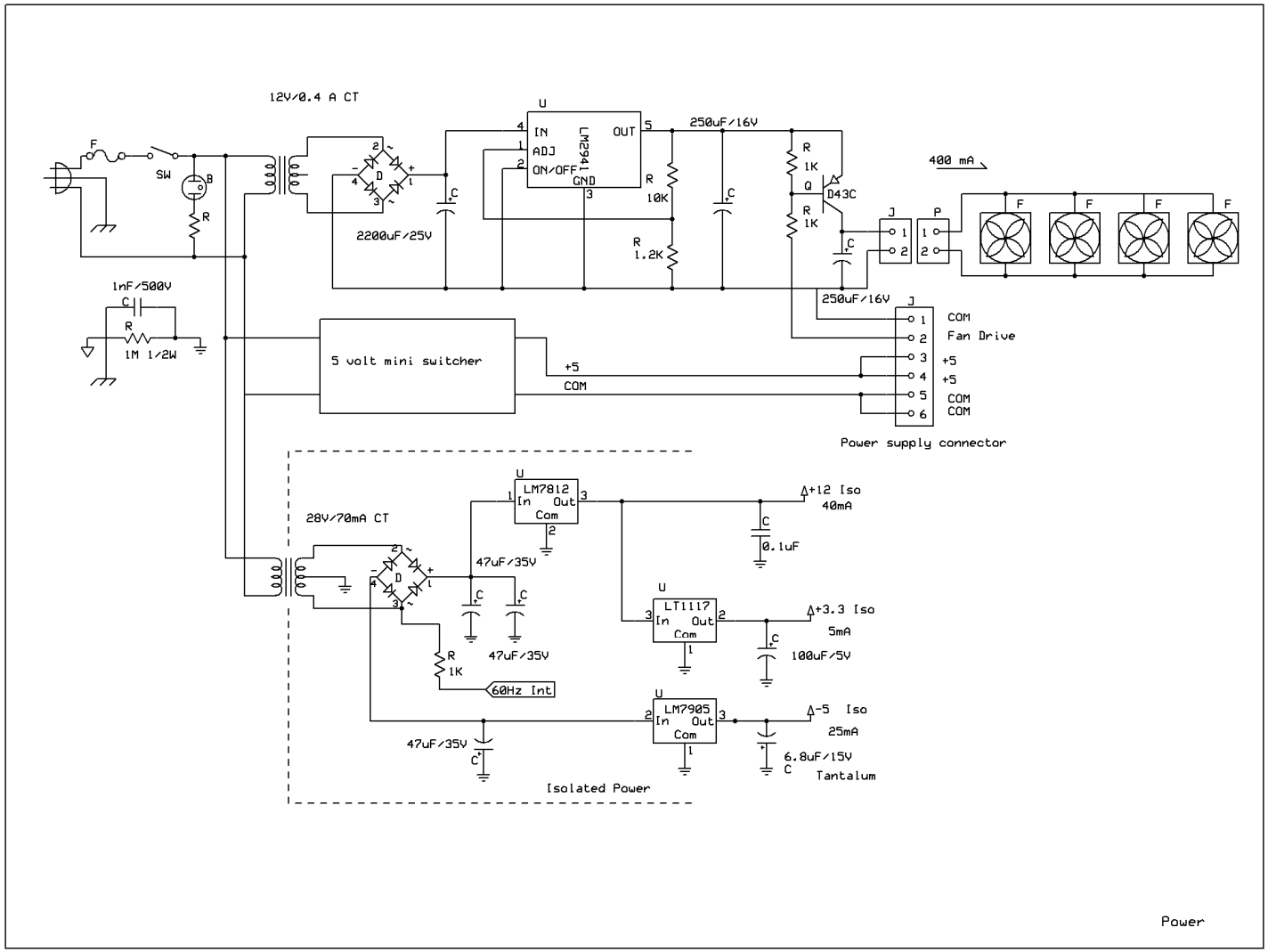
Current Sink



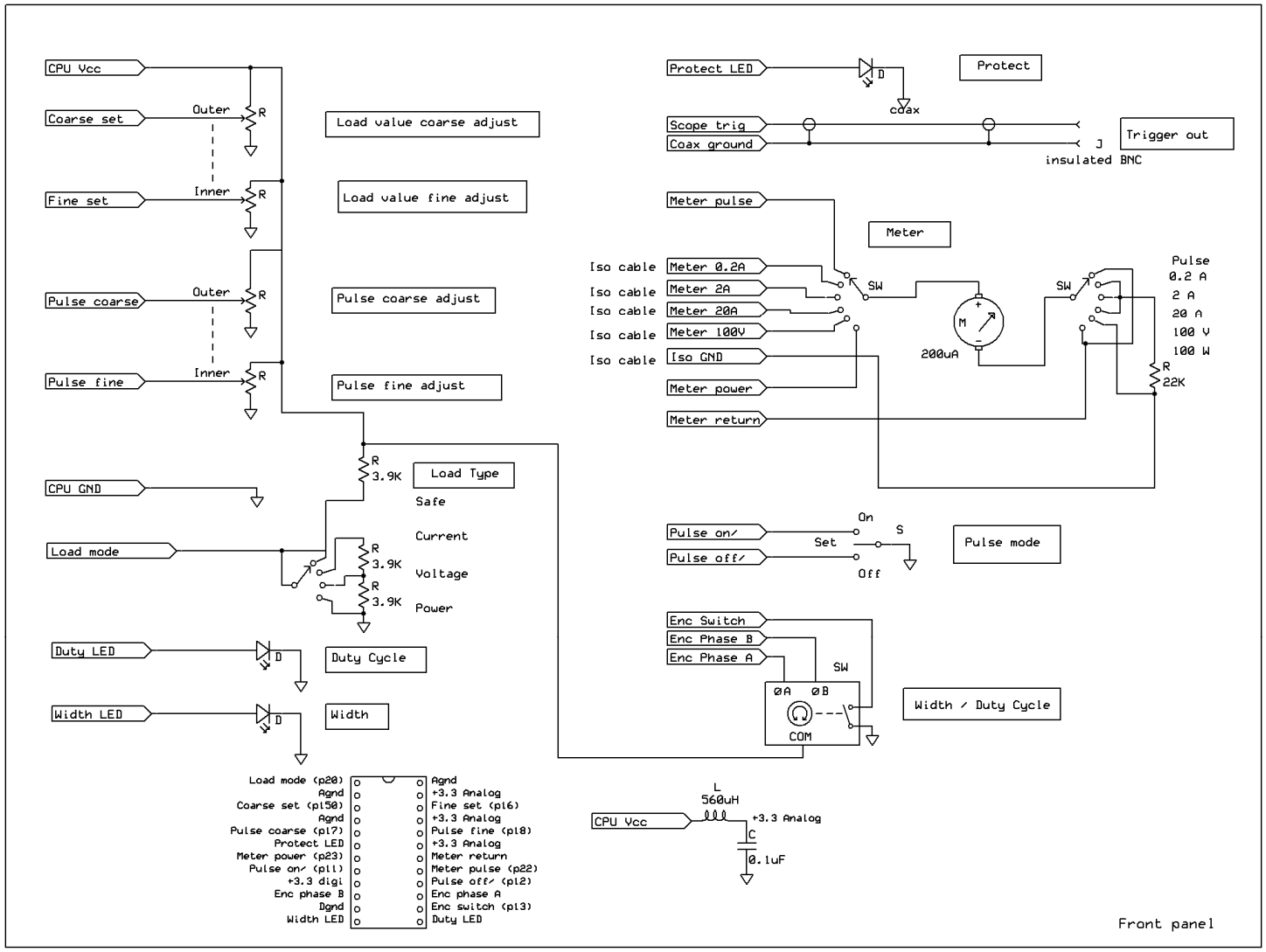
Volt/temp Monitor



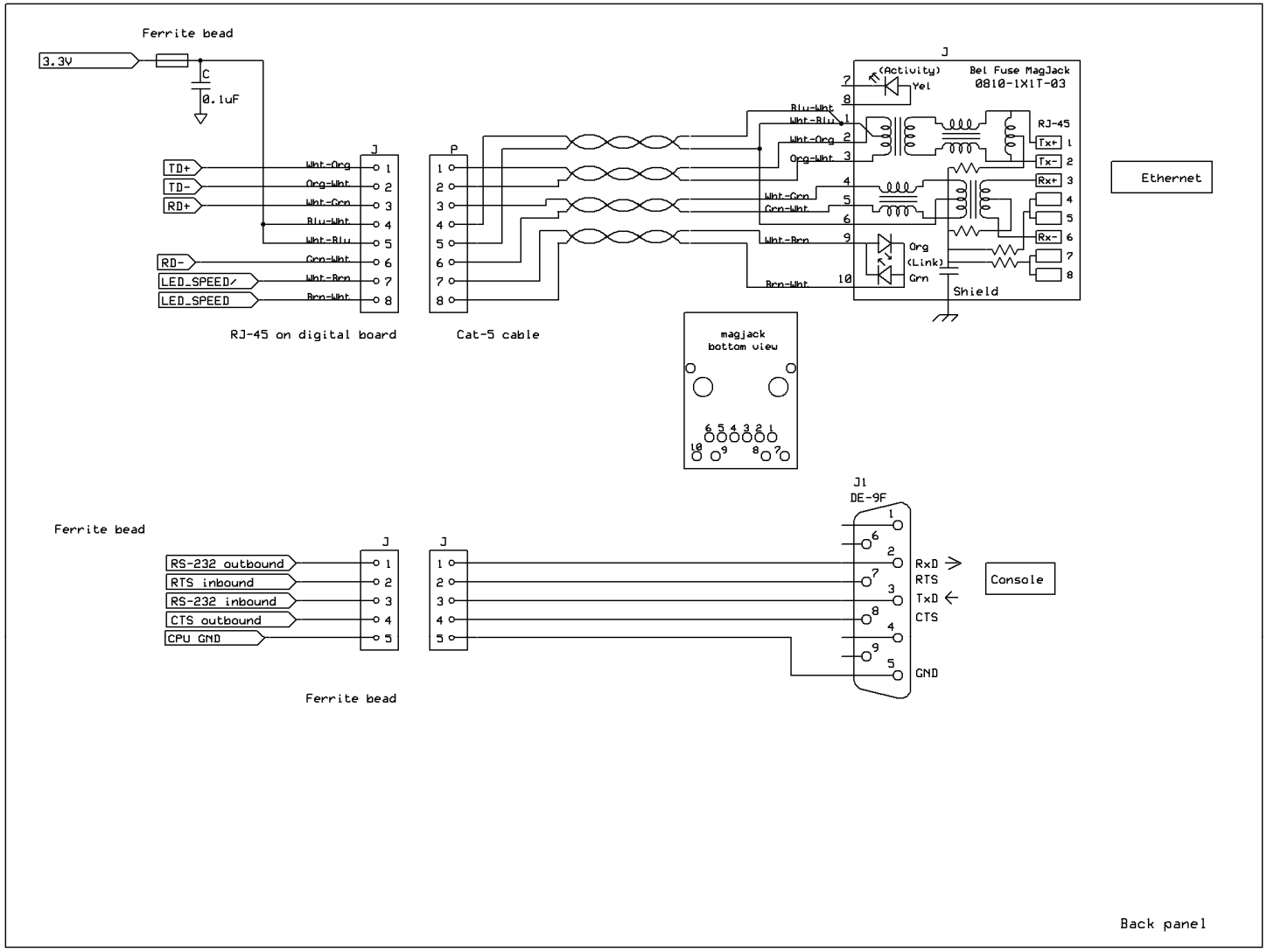
Power


12V/0.4 A CT
F
SW
B
R
2200uF/25V
U
IN
ADJ
ON/OFF
GND
OUT
LM2941
250uF/16V
R
10K
R
1.2K
R
1K
Q
D43C
R
1K
400 mA
J
P
F
F
F
F
250uF/16V
1nF/500V
C
R
1M 1/2W
5 volt mini switcher
+5
COM
J
COM
Fan Drive
+5
+5
COM
COM
Power supply connector
28V/70mA CT
U
LM7812
In Out
Com
+12 Iso
40mA
0.1uF
47uF/35V
47uF/35V
R
1K
60Hz Int
U
LT1117
In Out
Com
+3.3 Iso
5mA
100uF/5V
U
LM7905
In Out
Com
-5 Iso
25mA
47uF/35V
6.8uF/15V
Tantalum
Isolated Power
Power

Front Panel


CPU Vcc
Coarse set
Outer
R
Load value coarse adjust
Fine set
Inner
Load value fine adjust
Pulse coarse
Pulse coarse adjust
Pulse fine
Pulse fine adjust
CPU GND
Load mode
3.9K
Load Type
Safe
Current
Voltage
Power
Duty LED
Duty Cycle
Width LED
Width
Protect LED
Protect
coax
Scope trig
Coax ground
Trigger out
insulated BNC
Meter pulse
Meter
Iso cable
Meter 0.2A
Meter 2A
Meter 20A
Meter 100V
Iso GND
Meter power
Meter return
SW
M
200uA
22K
Pulse
0.2 A
2 A
20 A
100 V
100 W
Pulse on/
Pulse off/
On
Set
Off
S
Pulse mode
Enc Switch
Enc Phase B
Enc Phase A
ØA
ØB
COM
Width / Duty Cycle
Load mode (p20)
Agnd
Coarse set (pl50)
Pulse coarse (pl7)
Protect LED
Meter power (p23)
Pulse on/ (pl1)
+3.3 digi
Enc phase B
Dgnd
Width LED
Agnd
+3.3 Analog
Fine set (pl6)
Pulse fine (pl8)
Meter return
Meter pulse (p22)
Pulse off/ (pl2)
Enc phase A
Enc switch (pl3)
Duty LED
L
560uH
C
0.1uF
Front panel

Back Panel


Ferrite bead
3.3V
C
0.1uF
J
TD+
TD-
RD+
RD-
LED_SPEED/
LED_SPEED
Wht-Org
Org-Wht
Wht-Grn
Blu-Wht
Wht-Blu
Grn-Wht
Wht-Brn
Brn-Wht
RJ-45 on digital board
P
Cat-5 cable
Blu-Wht
Wht-Blu
Wht-Org
Org-Wht
Wht-Grn
Grn-Wht
Wht-Brn
Brn-Wht
J
(Activity)
Yel
Bel Fuse MagJack
0810-1X1T-03
RJ-45
Tx+
Tx-
Rx+
Rx-
Org
(Link)
Grn
Shield
Ethernet
magjack
bottom view
6 5 4 3 2 1
10 9 8 7
J1
DE-9F
Ferrite bead
RS-232 outbound
RTS inbound
RS-232 inbound
CTS outbound
CPU GND
RxD
RTS
TxD
CTS
GND
Console
Ferrite bead
Back panel

Module Interconnection